ABSTRACT

DATA DECODING

An arrangement for selecting the largest of a plurality of input currents (pma (k-1), pmb (k-1)) and adding a further current (Ibmk) to the selected current, the arrangement comprising: a plurality of inputs (901, 902) for receiving said input currents; a further input (905) for receiving said further current; an output (906, 907) for delivering an output current proportional to the sum of the largest of the input currents and the further current; means for feeding each of the received input currents to the main current conducting path of a respective transistor, (T900, T902) each of the transistors having its control electrode connected to a common point; a respective follower transistor (T901, T903) connected between the input and the common point; and a mirror transistor (T904) having its control electrode connected to the common point for producing a current whose value is related to that of the largest input current.

The currents through transistors (T904, T907) are summed and sensed by a diode connected transistor (T905) whose gate voltage is stored on a capacitor (C900, C901) by means of respective switches (S900, S901). The voltages across the capacitors (C900, C901) are fed via respective switches (S902, S903) to the gate electrodes of transistors (T908, T909) whose drain electrodes feed an output current (pmc (k-1)) to outputs (906, 907) of the arrangement.

A plurality of such arrangements are used for producing path metric currents for a Viterbi decoder.

(Figure 8.)